CLAIMS:

1. A circuit comprising:

a plurality of data input terminals each for receiving respective serial data signals having the same bit rate,

bit clock generating means responsive to the serial data signals to provide for each a respective bit clock signal aligned with that data signal and having a period equal to twice the bit period of the data signal,

bit clock phase adjustment means responsive to the relative phases of the bit clocks to adjust the phases of the bit clocks relative to one another so that they all lie within a common interval of 180° of phase, where 360° of phase represents the period of the bit clock.

2. A circuit as claimed in claim 1 wherein the plurality of bit clocks comprise a master one, the others of the plurality being slave ones, and the bit clock phase adjustment means is arranged to compare the master bit clock signal with the phase of the other or each of the other, slave, bit clock signals and to adjust the phase of the or each slave bit clock signal if it falls outside the common interval of 180° of phase.

3. A circuit as claimed in claim 2 wherein the adjustment means is such that the common interval is defined with respect to the phase of the master bit clock.

4. A circuit as claimed in claim 3 wherein the common interval is centred on the phase of the master bit clock.

5. A circuit as claimed in claim 1 wherein the phase adjustment means is arranged to adjust the phase of a bit clock signal that is outside the common interval to a phase that is defined with respect to the phase of the or a master one of the bit clock signals and that is within the common interval.

6. A circuit as claimed in claim 5, wherein the phase adjustment means is arranged to adjust the phase of a bit clock signal that is outside the common interval to be equal to the phase of the master bit clock signal.

7. A circuit as claimed in claim 6 wherein the bit clock generating means is arranged to re-align a bit clock signal to its associated serial data signal after the said adjustment of the phase.

8. A circuit as claimed in claim 1, wherein the phase adjustment means is arranged to adjust, by 180°, the phase of a bit clock signal outside the common interval.

9. A circuit as claimed in claim 8 comprising an inverter connected to be switched in or out of the path of a bit clock signal to perform the said 180° phase adjustment.

10. A circuit as claimed in claim 1 wherein a separate bit clock generating means is provided for each bit clock signal of the plurality and the bit clock phase adjustment means is provided as a centralised unit connected to receive from each separate bit clock generating means a signal representing the phase of its bit clock signal and to send to at least some of the

separate bit clock generating means signals indicating that an adjustment of the phase of its bit clock signal is to be made.

11. A circuit as claimed in claim 10 wherein one of the separate bit clock generating means provides a master phase, the centralised bit clock phase adjustment means is arranged to compare each of the phase signals from the other separate bit clock generating means with the master phase, and the centralised bit clock phase adjustment means is connectable to all of the separate bit clock phase adjustment means except the master one to provide them with signals indicating that an adjustment of phase is to be made.

12. A circuit as claimed in claim 10 wherein the separate bit clock generating means, or the said at least some of those, each comprise an inverter connected to be switched in or out of the path of the bit clock signal to perform a 180° phase adjustment on its bits clock signal.

13. A circuit as claimed in claim 1 wherein a separate bit clock generation means is provided for each bit clock signal of the plurality and a separate slave bit clock phase adjustment means is provided for all but a master one of the bit clock signals of the plurality, the slave bit clock phase adjustment means each being connected to receive the phase signal from the bit clock generation means of the master bit clock signal and being responsive thereto to adjust the phase of its bit clock signal.

14. A circuit as claimed in claim 1 wherein the bit clock phase adjustment means, or each said separate bit clock phase

adjustment means, comprises a phase comparator for performing the said comparison of the phases of the bit clocks.

15. A circuit as claimed in claim 14 wherein the phase comparator comprises a digital circuit responsive to digital signals representing the phases of the bit clock signals to perform the said comparing the phases of the bit clocks.

16. A circuit as claimed in claim 1 wherein the bit clock generating means, or each said bit clock generating means comprises a phase selector operative to store a digital phase value representing the phase of a bit clock signal, means responsive to that digital phase value to generate a bit clock signal of a corresponding phase.

17. A circuit as claimed in claim 16 wherein the bit clock generating means comprises an early/late detector operative to compare the phases of the bit clock and its associated data signal and to adjust the value stored in the phase selector so as to keep the bit clock in a particular phase relationship with its associated data signal.

18. A circuit as claimed in claim 16, wherein the bit clock phase adjustment means is operative to effect the said adjustment of the phase of the bit clock by adjusting the value in the phase selector.

19. A method receiving a plurality of parallel data signals of the same bit rate comprising:

generating for each data signal a respective bit clock signal aligned with that data signal and having a period equal to twice the bit period of the data signal, and

adjusting the phases of the bit clocks relative to one another so that they all lie within a common interval of 180° of phase, where 360° of phase represents the period of the bit clock.

20. A method as claimed in claim 19 comprising:

designating one of the said bit clocks as a master bit clock and the others as slave bit clocks,

comparing the phase of each of the slave bit clocks with that of the master bit clock, and

in response to that, adjusting each slave bit clock that falls outside said common interval of 180° of phase.

21. A method as claimed in claim 20 wherein the common interval is defined with respect to the phase of the master bit clock.

22. A method as claimed in claim 21 wherein the common interval is centred on the phase of the master bit clock.

23. A method as claimed in claim 19 wherein the adjusting of the phase of a bit clock signal that is outside the common interval is to a phase that is defined with respect to a, or the, master one of the bit clock signals and that is within the common interval.

24. A method as claimed in claim 23 wherein the adjusting of the phase of a bit clock signal that is outside the common interval is to a phase equal to that of the master bit clock signal.

25. A method as claimed in claim 24 comprising re-aligning a bit clock signal to its respective data signal after the said adjusting of the phase.

26. A method as claimed in claim 19 wherein the adjusting of a bit clock signal outside the common interval is by 180°.

27. A method as claimed in claim 20, wherein the generating and adjusting of the bit clock signals take place in separate units associated with the respective bit clock signals and the comparing is performed for all of the bit clock signals in a centralised unit that signals the separate units when to adjust the phase of the bit clock signals.

28. A method as claimed in claim 20, wherein the generating and adjusting of the bit clock signals takes place in separate units for each and the said comparing for a bit clock signal is performed in its unit also, each unit receiving the master bit clock signal for that comparing.